What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate of a first conductivity;

a first electrode formation region and a second electrode formation region formed adjacent to an inner surface of the semiconductor substrate,

wherein the first electrode formation regions and the second electrode formation regions are isolated from each other via an element isolation region,

an upper first-type impurity layer and a lower first-type impurity layer are formed in one of the first electrode formation region and the second electrode formation region,

the lower first-type impurity layer has a different first-type impurity concentration from the upper first-type impurity layer and is formed under the upper first-type impurity layer,

a second-type impurity layer and a first-type impurity layer are formed in the other electrode formation region and the first-type impurity layer is formed under a part of the second-type impurity layer having second-type impurities.

2. A semiconductor device according to Claim 1, wherein the upper first-type impurity layer formed in one of the electrode formation regions is set higher than the lower first-type impurity layer formed thereunder in first-type impurity concentration.

3. A semiconductor device comprising:

a semiconductor substrate of a P-type conductivity;

an anode electrode formation region and a cathode electrode formation region which are formed adjacent to an inner surface of the semiconductor substrate,

wherein the anode electrode formation region and a cathode electrode formation region are isolated from each other via an element isolation region,

in the anode electrode formation region a first P-type diffusion layer and a second P-type diffusion layer are formed inside the substrate in order of increasing proximity to the inner surface of the substrate,

the first P-type diffusion layer is higher than the second P-type diffusion layer in P-type impurity concentration;

in the cathode electrode formation region a first N-type diffusion layer and a third P-type diffusion layer are formed inside the substrate in order of increasing proximity to the inner surface of the substrate, and

the third P-type diffusion layer is formed locally in a region exclusive of the vicinity of the element isolation region inside the cathode electrode formation region.

4. A semiconductor device according to Claim 3, wherein the first P-type diffusion layer is formed in a region from the surface of the substrate to 0.4 μ m in depth, and the second P-type diffusion layer is formed in a region at a depth of 0.4 μ

m to a depth of 1.0 μ m below the surface of the substrate.

5. A semiconductor device according to Claim 3, wherein an anode electrode and a cathode electrode are formed in the anode electrode formation region and the cathode electrode formation region, respectively, on the semiconductor substrate and a diode formed of the anode electrode and the cathode electrode is used as a protection circuit for input/output terminals.

6. A method for manufacturing a semiconductor device comprising:

an element isolation step for forming element isolation regions at predetermined intervals so as to form an anode electrode formation region and a cathode electrode formation region apart from each other on a surface of a semiconductor substrate of a P-type conductivity;

a first implantation step for implanting N-type impurities into the cathode electrode formation region;

a second implantation step for implanting P-type impurities into the anode electrode formation region;

a third implantation step for implanting the P-type impurities throughout the anode electrode formation region and into a part of the cathode electrode formation region;

a thermal diffusion step for diffusing the implanted P-type and N-type impurities by an annealing treatment, and

an electrode formation step for forming an anode

electrode and a cathode electrode by accumulating metal material on the semiconductor substrate in the anode electrode formation region and the cathode electrode formation region by means of sputtering.

7. A method for forming a semiconductor device according to Claim 6, wherein an upper P-type impurity layer and a lower P-type impurity layer are formed inside the substrate in the anode electrode formation region after the third implantation step, and the upper P-type impurity layer is set higher than the lower P-type impurity layer formed thereunder in P-type impurity concentration.

8. A method of forming a semiconductor device according to Claim 6, wherein the P-type impurities to be implanted into the cathode electrode formation region in the third implantation step is implanted in a region in the cathode electrode formation region which is 0.5 μm or more apart from a portion in contact with the element isolation region.